<ISSCC2006 報告会>

日時： **2006年3月17日（金） 9:30-17:15**
会場： 東京大学本郷キャンパス 武田先端知ビル**5**階武田ホール
主催： **Japan Chapter, IEEE Solid-State Circuits Society**
協賛： **ISSCC Far-East Regional Committee**

<<午前の部>>

9:30-9:35 **Welcome**
Tadashi Shibata SSCS Japan Chapter Chair (University of Tokyo)

9:35-10:00 **ISSCC2005Overview**
Kunihiko Iizuka ISSCC Far East Region Chair (Sharp)

10:00-10:30 **(32.3) A PLL for a DVDx16 Write System with 63 Output Phases and 32ps Resolution**
Shiro Dosho(Matsushita)

10:30-11:00 **(19.3) A Digital Input Controller for Audio Class-D Amplifier with 100W 0.004% THD+N and 113dB Dynamic Range**
Toru Ido (Texas Instruments Japan)

11:00-11:30 **(28.5) A 1ps-Resolution Jitter-Measurement Macro Using Interpolated Jitter Oversampling**
Koichi Nose (NEC)

11:30-12:00 **(27.1) A 1/1.8" 6.4M Pixel, 60Frames/s CMOS Image Sensor with Seamless Mode Change**
Satoshi Yoshihara (Sony)

昼休み **12:00～13:00**

<<午後の部 **I**>>

13:00-13:30 **(7.7) A 56nm CMOS 99mm^2 8Gb Multi-level NAND Flash Memory with 10Mbyte/sec Program Throughput**
Ken Takeuchi (Toshiba)

13:30-14:00 **(34.5) Re-definition of Write margin for next-generation SRAM designs and Write margin monitoring circuit based on this definition**
Koichi Takeda (NEC)

14:00-14:20 **(29.4) Hierarchical Power Distribution with Power Tree in Dozens Power Domains for 90-nm Low-Power Multi-CPU SoCs**
Yusuke Kanno (Hitachi)

14:20-14:40 **(29.5) A Power Management Scheme Controlling 20 Power Domains for a One Chip Mobile Processor**
Toshihiro Hattori (Renesas Technology)

14:40-15:00 **(23.7) "System-in-Silicon" architecture and its application to an H.264/AVC motion estimation for 1080HDTV**
Kouichi Kumagai (System Fabrication Technologies)

休憩 **15:00 – 15:15**

<<午後の部 **II**>>

15:15-15:45 **(15.4) An Organic FET SRAM for Braille sheet display with back gate to increase the static noise margin**
Makoto Takamiya (University of Tokyo)

15:45-16:15 **(5.6) High Speed Interconnect for Multiprocessor Server using Over 1Tbits/s Crossbar LSI**
Jun Yamada (Fujistsu)

16:15-16:45 **(6.4) A 1.1V 3.1 to 9.5 GHz MB-OFDM UWB Transceiver in 90nm CMOS**
Akio Tanaka (NEC)

16:45-17:15 **(20.7) A 10.8mA Single Chip Transceiver for 430MHz Narrowband Systems in 0.15um CMOS**
George Hayashi (Matsushita Electric Industrial)

17:15 閉会

［お問い合せ先］

IEEE SSCS Japan Chapter Secretary： 藤島 実（**fuji@k.u-tokyo.ac.jp**）
Homepage: http://www.ieee-jp.org/japancouncil/chapter/SSC-37/ssc.htm